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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,010	12/13/2001	Scott Derner	400.119US01	2780

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,010	DERNER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/03/2005 have been fully considered but they are not persuasive.

The Applicant contends, "No embodiment of McConnell is without the redundancy and external hardware/processor for doing the actual work that is performed on-ship in the present claims".

The Examiner would like to point out that the Applicant's contention exclusive use of an "external hardware/processor for doing the actual work" is a fabrication of the Applicant. Nowhere in the McConnell patent does McConnell explicitly teach that the repair device is performed in **exclusively** in an external hardware/processor. In fact, col. 4, lines 2-5 refer to Figure 1 as a single integrated memory. The Authoritative Dictionary of IEEE Standards Terms defines integrated circuit as a combination of interconnected circuit elements inseparably associated on or within a continuous substrate, i.e., a chip. Furthermore, col. 9, lines 15-21 in McConnell explicitly teaches that Figure 4 in McConnell is a single processor for carrying out the functions of the redundancy detection device 4 and of the repair device 5 and col. 4, lines 59-61 in McConnell explicitly teaches that that the processor can be on the same integrated circuit as the integrated memory. McConnel recognizes both arrangements have utility. The Examiner asserts that one of ordinary skill in the art at the time the invention was made

would have recognized that on chip hardware offers faster operating speeds while off-chip hardware offers design flexibility, that is, motivation for use of either design is well known and ancient in the art.

The Applicant contends, "Barth, Jr., et al. is cited for adding on-chip ECC. However, as has been clearly shown above, the addition of on-chip ECC would substantially alter the principle of operation of McConnell et al".

The Examiner disagrees and asserts that McConnel teaches that ECC functions are carried out in the repair device 5 in McConnel. There is nothing in McConnel to preclude the repair device 5 in McConnel to be an on-chip device and there is every indication in McConnel as pointed out above that McConnel intended that an embodiment with an on-chip repair device 5 because: 1) col. 4, lines 2-5 refer to Figure 1 as a single integrated memory and The Authoritative Dictionary of IEEE Standards Terms defines integrated circuit as a combination of interconnected circuit elements inseparably associated on or within a continuous substrate, i.e., a chip; and 2) col. 9, lines 15-21 in McConnell explicitly teaches that Figure 4 in McConnell is a single processor for carrying out the functions of the redundancy detection device 4 and of the repair device 5 and col. 4, lines 59-61 in McConnell explicitly teaches that that the processor can be on the same integrated circuit as the integrated memory.

Barth, Jr., et al. explicitly teaches on-chip ECC. The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have recognized that

on chip hardware offers faster operating speeds while off-chip hardware offers design flexibility, that is, motivation for use of either design is well known and ancient in the art.

The Examiner disagrees with the applicant and maintains all rejections of claims 9-14 and 24-26. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 9-14 and 24-26 are not patentably distinct or non-obvious over the prior art of record in view of the references, McConnell; Roderick et al. (US 5986952 A, hereafter referred to as McConnell) in view of Barth, Jr.; John E. et al. (US 5134616 A, hereafter referred to as Barth) as applied in the last office action, filed 07/01/2005. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 9-14 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McConnell; Roderick et al. (US 5986952 A, hereafter referred to as McConnell) in view of Barth, Jr.; John E. et al. (US 5134616 A, hereafter referred to as Barth).

See the Non-Final Action filed 07/01/2005 for detailed action of prior rejections.

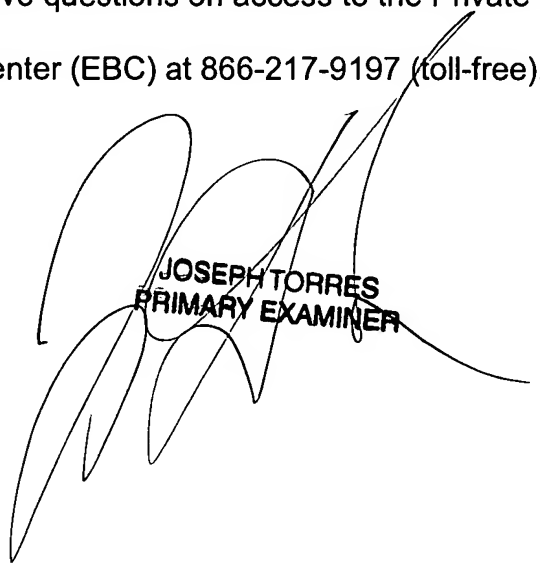
Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133